# A 5.4-Gbit/s Adaptive Continuous-Time Linear Equalizer Using Asynchronous Undersampling Histograms

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***Abstract*—We demonstrate a new type of adaptive continuous-time linear equalizer (CTLE) based on asynchronous undersampling histograms. Our CTLE automatically selects the optimal equalizing filter coefficient among several predetermined values by searching for the coefficient that produces the largest peak value in histograms obtained with asynchronous undersampling. This scheme is simple and robust and does not require clock synchronization for its operation. A prototype chip realized in 0.13-$\mu$m CMOS technology successfully achieves equalization for 5.4-Gbit/s $2^{31}-1$ pseudorandom bit sequence data through 40-, 80-, and 120-cm PCB traces and 3-m DisplayPort cable. In addition, we present the results of statistical analysis with which we verify the reliability of our scheme for various sample sizes. The results of this analysis are confirmed with experimental data.**

***Index Terms*—Adaptive equalization, asynchronous undersampling histogram, continuous-time linear equalizer (CTLE).**

## I. Introduction

As the data rate requirements for many wireline applications continuously increase, intersymbol interference due to channel bandwidth limitation becomes a serious problem in high-speed serial interfaces. In order to compensate the limited channel bandwidth, various types of equalizers are widely used. In addition, many applications require equalizers having adaptation ability that can provide optimal equalization for different channel conditions.

Various adaptive equalizers have been reported [1]–[7]. In the spectrum balancing method, adaptive equalization is achieved by comparing high- and low-frequency components of data power and generating feedback signals until the power spectrum is balanced [1], [2]. Although equalizer adaptation in this method can be realized independent of timing recovery, its implementation requires complicated analog circuits whose performance can be affected by process variations. Digital-signal processing using the least mean square or the zero-forcing algorithm can be also used for adaptive equalization [3], [4]. This provides flexibility and easy programmability, but speed limitation and complexity of the required analog-to-digital converter limit applicability of this scheme for high-speed applications.

One promising adaptive equalization technique is using an eye-opening monitor (EOM) [5]–[7]. The EOM evaluates data quality with periodic observations of the filter output and provides information about the equalizing filter performance. Using this information, the equalizer can determine the optimal filter conditions. For these methods, synchronous sampling clock circuits and high-speed comparators are essential. Moreover, it can be difficult to recover clock signals from the initially closed eye diagram, limiting its applicability.

We proposed a new type of adaptive continuous-time linear equalizer (CTLE) based on asynchronous undersampling histograms [8]. Our technique is based on indirect monitoring of data eye opening with histograms obtained from asynchronous undersampling and does not require any data timing information. It is simpler than any previously reported EOM-based adaptive equalizers and can operate with initially closed eyes. Compared to our initial report in [8], we provide in this brief more detailed explanation of our scheme as well as more measurement results. Furthermore, the results of our statistical analysis for the reliability of our scheme at various sample sizes are given.

This brief is organized as follows. After introduction in Section I, Section II explains the adaptive equalization algorithm, and Section III describes implementation of the prototype adaptive equalizer chip. Section IV gives measurement results, and Section V presents the results of statistical analysis for our scheme. Section VI concludes this brief.

## II. Asynchronous Undersampling Histogram

Our adaptation scheme is based on the simple observation that the clearest eye diagram produces the largest peak value in the histogram obtained with asynchronous undersampling. Fig. 1 shows sequences of random binary data with different amounts of equalization. When these are sampled with a clock which is asynchronous and slower than the data clock, different types of histograms are produced. For the case of overequalization, the equalizer output has enhanced high-frequency components, which tend to broaden the data amplitude distribution around peak values as shown in Fig. 2(a). For the case of underequalization, the distribution in the histogram is spread out as shown in Fig. 2(c). With optimal equalization, the distribution is concentrated at peak values as shown in Fig. 2(b). Based on these observations, we can easily determine the equalizer condition that results in the best eye quality by simply searching for the histogram that has the largest peak value.

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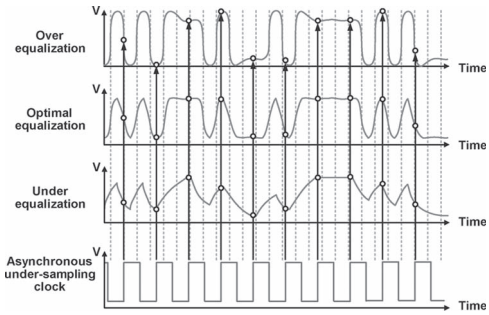


Fig. 1. Asynchronous undersampling process.

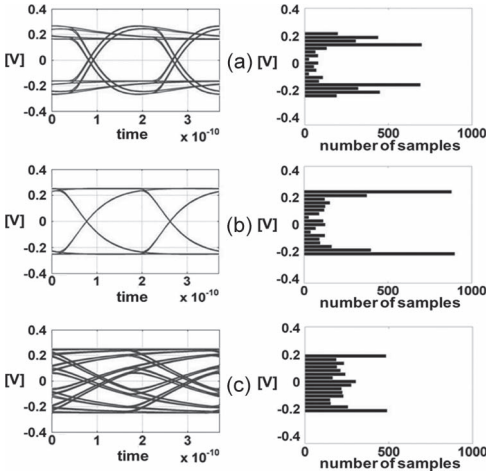


Fig. 2. Examples of eye diagrams and histograms: (a) Overequalization. (b) Optimal equalization. (c) Underequalization.

The histograms shown in Fig. 2 are obtained from Matlab simulation. The channel used for simulation is 3-m DisplayPort cable modeled with a three-pole low-pass filter whose characteristics are experimentally determined by $S$-parameter measurement of an actual cable. The poles are located at 1.061, 1.591, and 3.183 GHz. The equalizer used for simulation has a two-stage active filter in which high-frequency boosting is controlled by two zeros [1]. In the simulation, 5.4-Gbit/s $2^7 - 1$ pseudorandom bit sequence (PRBS) data are transmitted through the channel, and the eye diagrams resulting from three different filters having different amounts of high-frequency boosting are shown in Fig. 2. The resulting data are then asynchronously sampled with 114-MHz clock and compared with 32-amplitude levels for obtaining histograms. The sample size for each histogram is 4000.

In our scheme, the sampling clock is asynchronous to the transmitted data. In addition, asynchronous undersampling allows reliable data collection as long as a sufficient number of samples are taken and the sampling clock is not a subharmonic of the data clock. Such an asynchronous undersampling technique has been used for performance monitoring in optical communications [9].

With the aforementioned observations, we can easily realize an adaptive operation in which filter coefficients are scanned among several preset values and, for each case, an asynchronous undersampled histogram is obtained. Then, the optimal filter coefficient is selected as the one producing the histogram with the largest peak value. Our adaptive CTLE performs this operation.

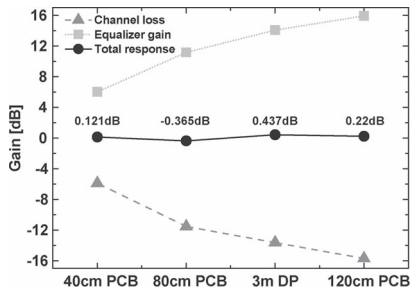


Fig. 3. Channel losses and corresponding optimal equalizer gains.

## III. Implementation

Our design target is 5.4-Gbit/s data transmission over 40-, 80-, and 120-cm PCB traces and 3-m DisplayPort cable. As the first step, we measured the channel characteristics using a network analyzer. The channels have from about 5.9- to 15.7-dB loss at 2.7 GHz as shown in Fig. 3. From this, we designed our adaptive CTLE to have from −4- to 18-dB equalizing gain which compensates channel loss as well as loss due to circuit implementation.

Fig. 4(a) shows the block diagram of our adaptive CTLE. It has an active equalizing filter with capacitive source degeneration and adaptive circuits which consist of four track-and-hold circuits, a comparator, two digital-to-analog converters (DACs), a clock generator, and a digital controller. The track-and-hold circuit is made up of pass-gate-logic with n-channel metal–oxide semiconductor (NMOS) and PMOS switches. The two-stage capacitive degeneration filter as shown in Fig. 4(b) contains a 4-bit NMOS resistor array, which provides 16 different levels of gain boosting with about 1.4-dB increment for channel-loss compensation.

The desired filter range and resolution was determined from Matlab simulation of the target channels with various filter conditions. The 5-bit DAC as shown in Fig. 4(c) generates 32-level reference voltages. The reference level is controlled from 600 mV to 1.2 V. The DAC resolution is 18.75 mV, which provides the desired filter coefficient resolution. The comparator as shown in Fig. 4(d) is a four-input differentially clocked sense amplifier and compares input data with DAC references. The comparator offset was confirmed less than 5 mV from postlayout simulation, which is less than the DAC resolution.

The clock generator as shown in Fig. 4(e) has a five-stage inverter chain and generates about 114-MHz five-phase clocks which are asynchronous to the target data rate. This sampling clock speed is chosen so that the prototype chip can be linked to a field-programmable gate array (FPGA), which allows external monitoring of histograms for a testing purpose. The five-phase sampling clocks are sequentially provided to the track-and-hold circuits, the comparator, and the digital controller. These multiphase clocks provide sufficient timing margins for comparator and counter, thus resulting in stable adaptation operation. The digital controller determines the histogram of received data amplitude for each filter coefficient setting and selects the coefficient that produces the histogram with the largest peak value.

The flow chart of adaptive equalization process is shown in Fig. 5. The controller is digitally synthesized and integrated on the chip. The adaptive equalization is performed as follows.

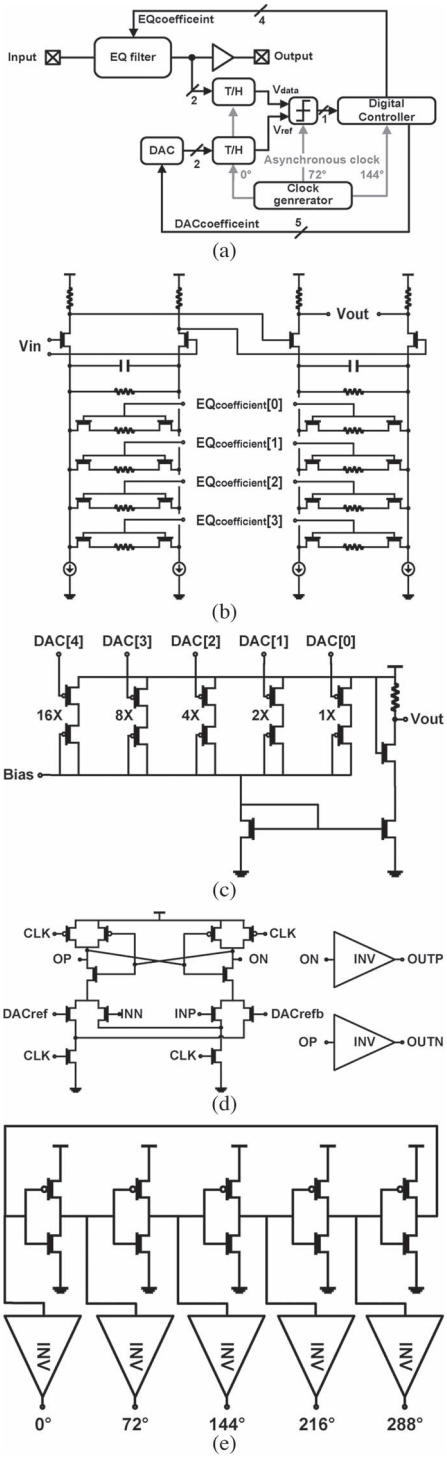


Fig. 4. (a) Block diagram of adaptive CTLE and schematics of (b) equalizing filter, (c) 5-bit DAC, (d) comparator, and (e) clock generator.

The filter coefficient is set to an initial value, and its output after passing track-and-hold circuit $V_{\rm data}$ is compared with the reference voltage $V_{\rm ref}$ produced the DAC. When $V_{\rm data}$ is larger than $V_{\rm ref}$, the comparator generates a high pulse, and the counter counts up. This is repeated for 4096 (12 bit) samples, and the register stores the counter value. Then, $V_{\rm ref}$ is increased to a new value, and the aforementioned sampling and counting process is repeated for 32 DAC coefficients, resulting in the cumulative distribution function (CDF). When this CDF is differentiated, a histogram for the given filter coefficient is

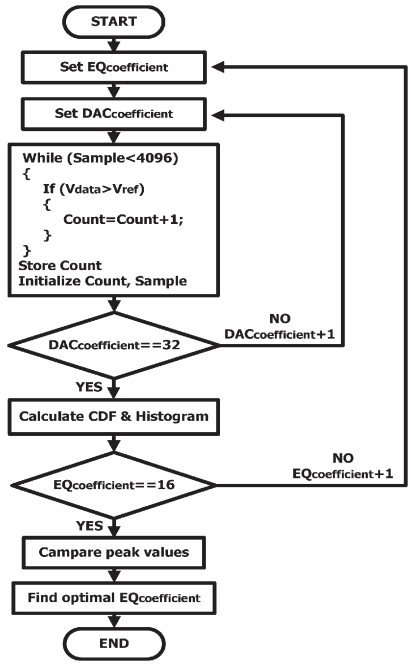


Fig. 5. Adaptive equalization process.

obtained. Then, this process is repeated for each of 16 (4 bit) filter coefficients. The controller determines the filter coefficient having the largest peak value and chooses this as the optimal equalizing filter coefficient.

Our controller produces 4096 samples with 12 bits. This sample size is determined by statistical analysis details of which are given in Section V. With this sample size, the total time required for determining the optimal filter coefficient can be estimated as follows:

$$4096\ (\text{sample number}) \times 32\ (\text{reference voltage number}) \times 16\ (\text{filter coefficient number}) \times 8.7\ \text{ns}\ (\text{time for each operation}) \sim 18\ \text{ms}. \quad (1)$$

It does take some time in order to determine the optimal filter coefficient for a given channel, but the fact that this scheme does not require any previous knowledge of the channel and relies on the digital block for adaptation makes it a promising solution for applications where the channel condition does not change once initial optimization is achieved.

## IV. Measurement

Fig. 6 shows a die photograph of our adaptive CTLE chip fabricated in 0.13-$\mu$m CMOS technology. The chip occupies less than 340 $\mu$m $\times$ 525 $\mu$m excluding the output buffer. Our adaptation circuits consume 26 mW and have 0.12-mm$^2$ area.

Fig. 7 shows the measurement setup where 5.4-Gbit/s PRBS $2^{31}-1$ data are generated by a pulse pattern generator and are fed to four different types of channels. The equalized output is observed by an oscilloscope. The integrated digital controller can be operated in internal- or external-control mode. In the external-control mode, histograms for different filter settings are delivered to FPGA for testing. In the internal-control mode, the digital controller sets the optimal filter coefficient as the one producing the histogram with the largest peak value.

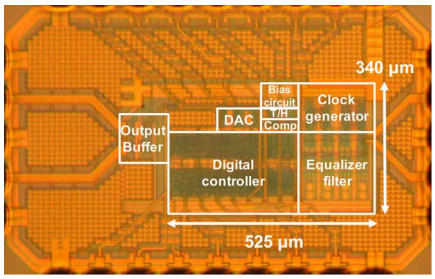


Fig. 6. Die photographs of prototype adaptive CTLE.

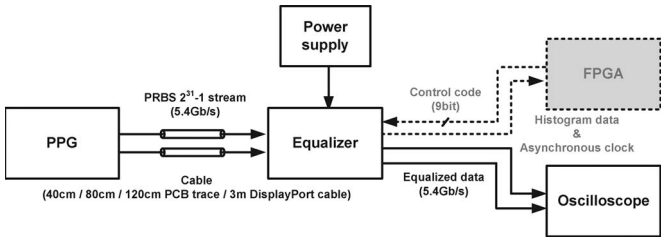


Fig. 7. Measurement setup.

Fig. 3 shows the channel response without any equalization for four different channels measured at 2.7 GHz by a network analyzer. It also shows the optimal boosting gain automatically provided by our adaptive CTLE. As shown in the figure, the total response is close to zero indicating that our adaptive CTLE provides the optimal amount of boosting gain that compensates channel loss for each of the four different channels.

Fig. 8 shows measured eye diagrams before and after equalization for four different channels with 5.4-Gbit/s $2^{31}-1$ PRBS data. As can be seen, all eyes are clearly open after equalization. The optimal filter coefficient for each case is adaptively determined by the circuit without any external control. The peak-to-peak jitters are 33.62, 34.81, 36.41, and 34.73 ps, respectively.

## V. Sample Size Analysis

A larger sample size guarantees better histogram reliability, but the sample size has limitation for practical implementation. In order to determine the proper sample size, we performed the following statistical analysis. For our analysis, we considered an eye diagram due to 3-bit random data sequence as shown in Fig. 9. Among all the possible data patterns, 111 data sequence always produces the high level when sampled, and both 011 and 110 sequences produce the high level half the time when sampled. The sampling process can be modeled with the binomial process in which the sampled data contributing to the high level are considered as success and all others are considered as failure. Consequently, when we sample a random 3-bit data sequence, the probability for sampling the high level $p$ is $(1+2\times 0.5)/8 = 1/4$. Here, 1/8 comes from 111 data sequence, and 0.5/8 comes from either 011 or 110.

The binomial process can be approximated by the normal distribution if $np > 10$ and $0.1 < p < 0.9$ [10], where $n$ represents the sample number. With this approximation, we can use the well-known properties of the normal distribution. The required minimum sample number $n$ with confidence interval

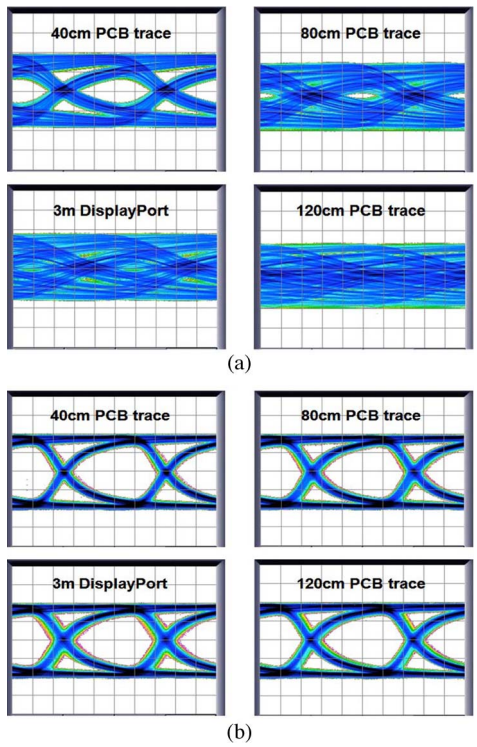


Fig. 8. Eye diagrams of (a) before and (b) after equalization [(a) $X$: 37 ps/div, $Y$: 100 mV/div; (b) $X$: 37 ps/div, $Y$:100 mV/div].

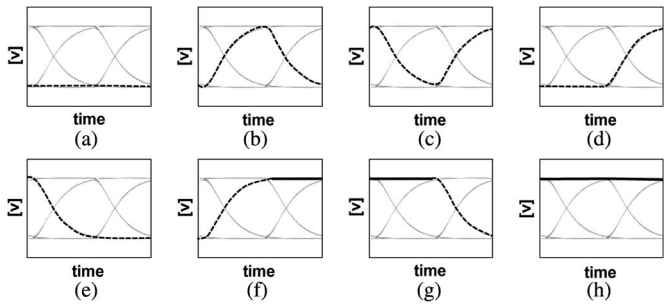


Fig. 9. (Straight line) Probability of success for 3-bit data pattern. (a) 000; (b) 010; (c) 101; (d) 001; (e) 100; (f) 011; (g) 110; (h) 111.

of $(1-\alpha)$ resulting in $p$ bounded by $p-e$ and $p+e$, where $e$ represents the margin of error, is given as [11]

$$n = \frac{p(1-p)(z_{1-\alpha/2})^2}{e^2}. \tag{2}$$

Here, $z_{1-\alpha/2}$ is the critical value in the normal distribution with probability of $\alpha/2$ in each tail. For example, for 99% confidence interval, $\alpha$ is 0.01, and $z_{1-\alpha/2}$ is 2.58. We found from our simulation that $e = 0.0175$, or 1.75% margin of error, guarantees a sufficient difference between the largest and the second largest peak values in our histograms. With 99% confidence interval and 1.75% margin of error, the minimum sample size determined by (2) is 4075.

To verify reliability of our scheme, we measured in the external-control mode the peak value of the optimal histogram for each channel with varying sample sizes. The sample size was varied from 500 to 7000 in increment of 1000. Measurement at each sample size was repeated 100 times, and their averages and variances were determined. Here, the results

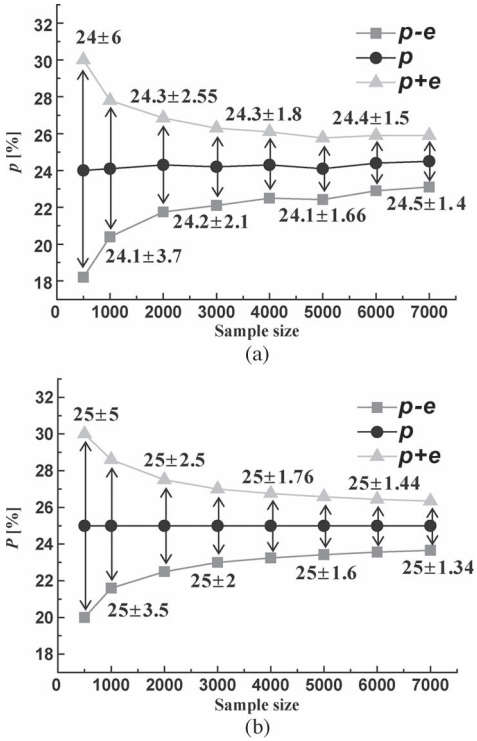


Fig. 10. (a) Measured $p$ and $e$ of 40-cm PCB trace and (b) calculated $p$ and $e$ for different sample sizes.

correspond to $p$ and the variance $e$. Fig. 10(a) shows measured $p$ and $e$ for 40-cm PCB trace for different sample sizes. As expected, measured $e$ decreases as the sample size increases. When the sample size is larger than 4000, measured $e$ is less than 1.8%. Fig. 10(b) shows the calculated $p$ and $e$ for different sample sizes. There is a good agreement between the results shown in Fig. 10(a) and (b), confirming accuracy in our analysis. Measurement results from other channel types showed the similar result.

## VI. Conclusion

We have demonstrated a new adaptive CTLE using asynchronous undersampling histograms. Using an asynchronous undersampling clock, data amplitude histograms are obtained at various equalizing filter coefficient settings, and the one producing the histogram with the largest peak value is selected as the optimum coefficient. With a prototype chip fabricated in 0.13-$\mu$m CMOS technology, we successfully equalized 5.4-Gbit/s data transmitted through 40-, 80-, and 120-cm PCB traces and 3-m DisplayPort cable. In addition, we experimentally confirmed the reliability of our sampling method. We believe that our adaptive CTLE is simpler than any previously reported EOM-based equalizers because it eliminates high-speed clock paths, reduces the number of required samplers, and eliminates phase rotator circuitry. Consequently, it has great advantages in power consumption and chip size.

Table I shows performance summary of our adaptive CTLE in comparison with other previously reported EOM-based equalizers. Although a direct comparison of power consumption and chip size is not possible due to different data rates, we believe that our adaptive CTLE can be easily extended to 10-Gbit/s operation while maintaining its advantages of small power consumption and chip size.

TABLE I
Performance Comparison of the Proposed Equalizer

| | [5]* | [6]* | [7]** | This Work*** |
|---|---|---|---|---|
| Year | 2005 | 2009 | 2010 | 2011 |
| Process | CMOS 0.13 µm | CMOS 0.18 µm | CMOS 65 nm | CMOS 0.13 µm |
| Signal quality monitoring | Sync. 2-D EOM | Sync. 2-D EOM | 1-D EOM | Async. amplitude histogram |
| Adaptive equalization | Not Implemented | Not Implemented | Off-Chip monitoring | On-Chip monitoring |
| Data rate | 12.5 Gb/s | 10 Gb/s | 10 Gb/s | 5.4 Gb/s |
| Sampling clock speed | 12.5 GHz | 10 GHz | N/A | 114 MHz |
| Power consumption | 330 mW* | 171 mW* | 302 mW** | 35 mW*** |
| Chip area | 0.26 $mm^2$* | 0.06 $mm^2$* | 0.23 $mm^2$** | 0.18 $mm^2$*** |

*: contains only eye-opening monitoring circuit without equalizing filter
**: off-chip PDF extraction
***: includes integrated digital controller

## Acknowledgment

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